REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1, 3-16 and 18-24 are pending in the present application. Claims 1, 14-16 and 20-23 have been amended, Claims 2 and 17 have been canceled and Claim 24 has been added by the present amendment.

In the outstanding Office Action, Claims 20-23 were rejected under 35 U.S.C. §112, first paragraph; Claims 2 and 14 were rejected under 35 U.S.C. §112, second paragraph; Claims 1, 4, 16, 18, 20 and 23 were rejected under 35 U.S.C. §102(b) as anticipated by Minami et al; Claims 15-17, 22 and 23 were rejected under 35 U.S.C. §102(b) as anticipated by Taguchi; Claim 13 was allowed; and Claims 5 and 19 were indicated as allowable if rewritten in independent form.

Applicants thank the Examiner for the indication of allowable subject matter and for the courtesy of an interview extended to Applicants' representative on March 26, 2002. During the interview, the differences between the present invention and the applied art were discussed. No agreement was reached pending the Examiner's further review when a response is filed. Arguments presented during the interview are reiterated below.

Regarding the rejection of Claims 20-23 under 35 U.S.C. §112, first paragraph, the outstanding Office Action states the specification does not disclose a single element formed in the first well as claimed in Claims 20-23. Applicants note Claims 20-21 and 23 have been amended to recite that each of the first wells comprises a single element (Claim 22 has been cancelled). This feature is described at page 11, line 7, which states "[a] single element (e.g., an MOS transistor) is formed in a single first region R1." Accordingly, it is respectfully requested this rejection be withdrawn.

Further, regarding the rejection of Claims 2 and 14 under 35 U.S.C. §112, second paragraph, the corresponding subject matter has been amended to recite that the first and second wells of the first and second regions on one side with reference to a predetermined boundary are of a first conductivity type, and the first wells on the other side are of a second conductivity type (and not to recite that the first and second wells on the other side are of a second conductivity type). Note independent Claims 1 and 16 have been amended to include this subject matter. These features are clearly shown in Figure 24, for example, in which the first wells W1 on the left side of the predetermined boundary BL are of a second conductivity type (e.g., n-type). Accordingly, it is respectfully requested this rejection be withdrawn.

Claims 1, 4, 16, 18, 20 and 23 stand rejected under 35 U.S.C. §102(b) as anticipated by Minami et al. This rejection is respectfully traversed.

As note above, independent Claims 1 and 16 have been amended to recite that the first and second wells of the first and second regions on one side with reference to a predetermined boundary are of a first conductivity type, and the first wells on the other side are of a second conductivity type.

For example, as shown in Figure 24, a second well W2 is formed in a second region R2 deeper than each of the first wells W1 in the semiconductor substrate 100. Further, the first and second wells W1, W2 of the first and second regions R1, R2 on one side with reference to the predetermined boundary BL are of a first conductivity type (e.g., p-type), and the first wells W1 on the other side of the predetermined boundary BL are of a second conductivity type (e.g., n-type).

This differs from Minami et al, which illustrates a first well 306 having a different conductivity than a second well 305 on one side with reference to a predetermined boundary (see Figure 36). That is, in Minami et al, the first and second wells of the first and second

regions on one side with reference to the predetermined boundary are not of a first conductivity type.

Accordingly, it is respectfully submitted independent Claims 1 and 16 and each of the claims dependent therefrom patentably define over Minami et al.

Claims 15-17, 22 and 23 stand rejected under 35 U.S.C. §102(b) as anticipated by Taguchi. This rejection is respectfully traversed.

Independent Claims 1 and 16 have also been amended to recite that the second well formed in the second region is deeper than each of the first wells in the semiconductor substrate. For example, as shown in Figure 24, the second well W2 is formed in a second region R2 deeper than each of the first wells W1 in the semiconductor substrate 100. This differs from Figure 3 in Taguchi which clearly shows the second well 12A formed in a second region is not deeper than each of the first wells 72 and 73 (see Figure 3).

In addition, independent Claim 15 has been amended to recite that the second well has a higher concentration than the first wells and is in contact with a plurality of the first wells. This feature distinguishes over Taguchi because the first and second wells (corresponding to the upper and lower portions of 73, respectively) in Taguchi have the same concentration.

Accordingly, it is respectfully submitted independent Claims 1, 15 and 16 and each of the claims depending therefrom also patentably defines over Taguchi.

Further, new Claim 24 has been added to set forth the invention in a varying scope, and is supported at least by Figures 2, 9, 10 and 15. In particular, new Claim 24 depends on Claim 15 and recites that the second wall is in contact with all of the first walls.

Consequently, in light of the above discussion and in view of present amendment, the present application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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IN THE CLAIMS

Please cancel Claims 2 and 17 without prejudice.

Please amend Claims 1, 14-16 and 20-23 as follows:

1. (Twice Amended) A semiconductor device comprising:

a semiconductor substrate;

an element isolation film formed such as to have a predetermined depth from a main surface of said semiconductor substrate, said element isolation film dividing the area from said main surface to said depth into a plurality of first regions;

first wells formed in said first regions, respectively; and

a second well formed in a second region deeper than each of said first wells in said semiconductor substrate, said second well being in contact with some of said first wells to provide electrical connection therebetween and not being in contact with said first wells adjacent to said some of said first wells,

wherein said first and second wells of said first and second regions on one side with reference to a predetermined boundary are of a first conductivity type, and said first wells on the other side are of a second conductivity type.

14. (Amended) A semiconductor device according to claim 13, wherein said first and second wells of said first and second regions on one side with reference to the predetermined

boundary are of a first conductivity type, and said first [and second] wells on the other side are of a second conductivity type.

15. (Amended) A semiconductor device comprising:

a semiconductor substrate;

an element isolation film formed such as to have a predetermined depth from a main surface of said semiconductor substrate, said element isolation film dividing the area from said main surface to said depth into a plurality of first regions;

first wells formed in said first regions, respectively; and

a second well formed in a second region deeper than said first wells in said semiconductor substrate, said second well having a higher concentration than said first wells and being in contact with [some] a plurality of said first wells,

wherein said first and second wells of said first and second regions on one side with reference to a predetermined boundary are of a first conductivity type, and said first and second wells on the other side are of a second conductivity type.

16. (Amended) A semiconductor device comprising:

a semiconductor substrate;

a plurality of element isolation films formed such as to have a predetermined uniform depth from a main surface of said semiconductor substrate, said element isolation films dividing the area from said main surface to said depth into a plurality of first regions;

first wells formed in said first regions, respectively; and

a second well formed in a second region deeper than each of said first wells in said semiconductor substrate, said second well being in contact with some of said first wells.

wherein said first and second wells of said first and second regions on one side with reference to a predetermined boundary are of a first conductivity type, and said first wells on the other side are of a second conductivity type.

20. (Amended) A semiconductor device according to claim 1, wherein each of the first wells [has] comprises a single element [formed therein].

21. (Amended) A semiconductor device according to claim 13, wherein each of the first wells [has] comprises a single element [formed therein].

22. (Amended) A semiconductor device according to claim 15, wherein each of the first wells comprises a single element.

23. (Amended) A semiconductor device according to claim 16, wherein each of the first wells [has] comprises a single element [formed therein].

24. (New).